

REMARKS

In the non-final Office Action, the Examiner rejected claims 1-57 under 35 U.S.C. § 103(a) as unpatentable over Kovacevic et al. (U.S. Patent No. 6,674,805) in view of Echeita et al. (U.S. Patent No. 6,078,958).

By this Amendment, Applicants add new claims 58-61. Applicants respectfully traverse the Examiner's rejection under 35 U.S.C. § 103. Claims 1-61 are pending.

In paragraphs 2-23 of the Office Action, the Examiner rejected claims 1-57 under 35 U.S.C. § 103(a) as allegedly unpatentable over Kovacevic et al. in view of Echeita et al. Applicants respectfully traverse the rejection.

Independent claim 1, for example, is directed to a system for processing data received in a plurality of incoming streams of variable speeds. The system comprises a memory configured to store data associated with a plurality of incoming streams of variable speeds, an interface controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory, and a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read the data from the memory.

Neither Kovacevic et al. nor Echeita et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 1. For example, Kovacevic et al. and Echeita et al. do not disclose or suggest a memory configured to store data associated with a plurality of incoming streams of variable speeds. In fact, Kovacevic et al. and Echeita et al. are completely silent with regard to streams of variable speeds.

The Examiner alleged that Kovacevic et al. discloses a memory configured to store data associated with a plurality of incoming streams of variable speeds and cited column 25, lines 21-

25, of Kovacevic et al. for support (Office Action, paragraph 2). Applicants respectfully disagree.

At column 25, lines 21-27, Kovacevic et al. discloses:

Because the private data from be transport packet has a variable length, there is no guarantee that the private data will end on a double word boundary. If the private data does not end on a double word boundary, the partial double word portion of private data at the end will not be sent to the FIFO until additional private data from unrelated source is received.

In this section, Kovacevic et al. discloses that private data from a transport packet has a variable length. Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest a memory configured to store data associated with a plurality of incoming streams of variable speeds, as required by claim 1.

Contrary to the Examiner's allegation, variable length packet data is not equivalent to streams of variable speeds. A stream speed is often defined in terms of how much data the stream can transmit per second. For example, a stream may have a speed of STS-3/OC-3 (e.g., approximately 155 Mbps) or STS-192/OC-192 (e.g., approximately 10,000 Mbps). In this case, data transmitted on the stream is transmitted at a speed of 155 Mbps or 10,000 Mbps, regardless of whether the data is associated with small packets, large packets, or variable-size packets. Accordingly, the Examiner's allegation lacks merit.

In response to a similar argument by Applicants, the Examiner simply quoted column 25, lines 20-23, of Kovacevic et al. (reproduced above) with no explanation of how this section of Kovacevic et al. could reasonably be construed to correspond to a memory configured to store data associated with a plurality of incoming streams of variable speeds, as required by claim 1 (Office Action, paragraph 24). If the Examiner persists with this rejection, Applicants

respectfully request that the Examiner provide a reasonable explanation of how the above-cited portion of Kovacevic et al. discloses or suggests a memory configured to store data associated with a plurality of incoming streams of variable speeds, as required by claim 1. If the Examiner cannot provide a reasonable explanation, then the Examiner must withdraw the rejection.

Kovacevic et al. and Echeita et al. also do not disclose or suggest an interface controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory, as further recited in claim 1. The Examiner admitted that Kovacevic et al. does not disclose this feature (Office Action, paragraph 2). The Examiner also alleged that Kovacevic et al. discloses this feature and cited column 19, lines 36-46, of Kovacevic et al. for support (Office Action, paragraph 25). Applicants respectfully disagree.

At column 19, lines 36-46, Kovacevic et al. discloses:

In operation, the System FIFO controller 466 provides an interface between the Parsers of FIGS. 5 and 7 and the FIFO 462. The controller 460 allows filtered packet data to be received and stored in the FIFO 462. Once stored in the FIFO 462, the System HBI controller 463 requests access to the video memory 471 through the controller 468. The controller 468 may include a system bus controller, a memory controller, or a combination of a memory/system bus controller. Generally, the controller 468 will control access to other system resources as well.

In this section, Kovacevic et al. discloses that system FIFO controller 466 allows filtered packet data to be received and stored in FIFO 462. Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest an interface controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory, as required by claim 1.

If the Examiner persists with this rejection, Applicants respectfully request that the Examiner provide a reasonable explanation of how the above-cited portion of Kovacevic et al.

discloses or suggests an interface controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory, as required by claim 1. If the Examiner cannot provide a reasonable explanation, then the Examiner must withdraw the rejection.

Presumably also with regard to this feature, the Examiner alleged that Echeita et al. discloses:

The media concentrator with arbitration 20 determines that the information of data streams one, two and three should be transmitted over e.g. a representative 30 Mbps available bandwidth channel to subscribe stations along with live data at a particular time, based on priority. The first frame of processed data of data stream two is placed on output of storage device

and cited column 7, line 64 - column 8, line 2, of Echeita et al. for support (Office Action, paragraph 2).

Applicants respectfully submit that the Examiner has not addressed the feature of claim 1. Claim 1 does not recite determining that three data streams should be transmitted over a 30 Mbps available bandwidth channel to subscribe stations based on priority. Instead, claim 1 recites an interface controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory. No reasonable argument can be made that the above-identified section of Echeita et al. discloses or remotely suggests this feature of claim 1.

If the Examiner persists with this rejection, Applicants respectfully request that the Examiner provide a reasonable explanation of how the above-cited portion of Echeita et al. discloses or suggests an interface controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory, as required by claim 1. If

the Examiner cannot provide a reasonable explanation, then the Examiner must withdraw the rejection.

Kovacevic et al. and Echeita et al. also do not disclose or suggest a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read the data from the memory, as further recited in claim 1. The Examiner alleged that Kovacevic et al. discloses a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds and configured to read the data from the memory using the second arbitration element and cited column 19, lines 47-61, of Kovacevic et al. for support (Office Action, paragraph 2). Applicants respectfully disagree.

At column 19, lines 47-61, Kovacevic et al. discloses:

In accordance with the invention, the System Memory 472 has been partitioned by the system host to include one or more system circular buffers 501-503. The system buffers 501-503 are implemented as circular buffers and are filled by operation of the controller 483. The controller 483 handles the buffer "write" pointer. The "read" pointer for the buffers is managed by the software on the system host side (not shown) which retrieves data from the buffers 501-503. There can also be a "high water" mark register associated with each buffer (not shown). The purpose of a "high water" mark register is to provide an interrupt when the write pointer crosses the value in this register. However, because there is generally only one interrupt for each of the plurality of buffers, software polling can be used to determine the cause of the interrupt.

In this section, Kovacevic et al. discloses that system memory 472 is partitioned into one or more circular buffers 501-503 and data is read from buffers 501-503 based on a read pointer managed by software on the system host side. Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read the data from the memory, as required by claim 1.

If the Examiner persists with this rejection, Applicants respectfully request that the Examiner provide a reasonable explanation of how the above-cited portion of Kovacevic et al.

discloses or suggests a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read the data from the memory, as required by claim 1. If the Examiner cannot provide a reasonable explanation, then the Examiner must withdraw the rejection.

For at least these reasons, Applicants submit that claim 1 is patentable over Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination. Claims 2-20 depend from claim 1 and are, therefore, patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claim 1. Claims 2-20 are also patentable over Kovacevic et al. and Echeita et al. for reasons of their own.

For example, claim 4 recites that the first arbitration element is configured to store a plurality of entries, where each of the entries includes a stream number that identifies one of the streams. Kovacevic et al. and Echeita et al. do not disclose or suggest the combination of features recited in claim 4.

The Examiner alleged that Kovacevic et al. discloses a first arbitration element that is configured to store a plurality of entries, where each of the entries includes a stream number that identifies one of the streams and cited column 16, lines 1-11, of Kovacevic et al. for support (Office Action, paragraph 5). Applicants respectfully disagree.

At column 16, lines 1-11, Kovacevic et al. discloses;

In the implementation of FIG. 21, a storage location within the storage locations 751 is reserved for the STREAM ID header field of a transport stream packet. In the embodiment shown at FIG. 21, inputs of the storage location for STREAM ID are connected to the appropriate bits of the data bus and the counter controller 752, to receive stream ID data from the FRAMER DATA representation of the transport stream at the correct time. The counter controller 752 receives the VSTART signal indicating

the start of a new video PES and generates enable signals to capture the stream ID, and other information, from the video PES header.

In this section, Kovacevic et al. discloses that there is a storage location for storing a STREAM ID header field. Nowhere in this section, or elsewhere, does Kovacevic et al. disclose or suggest a first arbitration element that is configured to store a plurality of entries that each includes a stream number that identifies one of the streams, where the first arbitration element arbitrates among the streams of variable speeds to store the data in the memory, as required by claim 4.

In response to a similar argument by Applicants, the Examiner alleged that Kovacevic et al. discloses the features of claim 4 at column 29, lines 59-63 (Office Action, paragraph 26).

Applicants disagree.

At column 29, lines 59-63, Kovacevic et al. discloses:

Referring to FIG. 16, the VIDEO PID storage location 424 provides the PID value which identifies the current video stream, while the shadow register associated with location 424 (not illustrated) stores the PID value of the next video stream to be accessed at the splice point.

In this section, Kovacevic et al. discloses that a PID value identifies a current video stream. Nowhere in this section, or elsewhere, however, does Kovacevic et al. disclose or suggest a first arbitration element that is configured to store a plurality of entries that each includes a stream number that identifies one of the streams, where the first arbitration element arbitrates among the streams of variable speeds to store data in the memory, as required by claim 4.

If the Examiner persists with this rejection, Applicants respectfully request that the Examiner provide a reasonable explanation of how the above-cited portion of Kovacevic et al. discloses or suggests a first arbitration element that is configured to store a plurality of entries that each includes a stream number that identifies one of the streams, where the first arbitration

element arbitrates among the streams of variable speeds to store data in the memory, as required by claim 4. If the Examiner cannot provide a reasonable explanation, then the Examiner must withdraw the rejection.

For at least these additional reasons, Applicants submit that claim 4 is patentable over Kovacevic et al. and Echeita et al. Claims 5-8 depend from claim 4 and are, therefore, also patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claim 4.

In addition, claim 5 recites that the number of entries in the first arbitration element for a particular one of the streams is based on a speed of the stream. Kovacevic et al. and Echeita et al. do not disclose or suggest the combination of features recited in claim 5.

The Examiner alleged that Kovacevic et al. discloses that the number of entries in the first arbitration element for a particular one of the streams is based on a speed of the stream and cited column 31, lines 10-21, of Kovacevic et al. for support (Office Action, paragraph 6). Applicants respectfully disagree.

At column 31, lines 10-21, Kovacevic et al. discloses;

FIGS. 39-42 illustrate a specific implementation of a method for blind synchronization to a transport stream. Blind synchronization allows the framer to acquire the transport stream, i.e. lock onto the transport stream, without any prior knowledge of the transport stream characteristics.

As discussed with reference to FIGS. 8 and 9, the transport stream can include a variety of signals. At a minimum, the transport stream will include a data signal (TDATA) and a clock signal (TCLOCK). Additional signals that may exist include TSTART, TVALID, and TERROR. Based upon these signals, the transport stream has a number of characteristics, such as individual signal polarities, and data ordering.

Contrary to the Examiner's allegation, there is nothing in this section of Kovacevic et al. that discloses or remotely suggests a first arbitration element with a number of entries for a particular one of the streams based on a speed of the stream, as required by claim 5.

The Examiner did not address these arguments when Applicants previously presented them. If the Examiner maintains the rejection of claim 5 based on Kovacevic et al., Applicants respectfully request that the Examiner identify where Kovacevic et al. or Echeita et al. discloses the features of claim 5 or identify claim 5 as allowable.

For at least these additional reasons, Applicants submit that claim 5 is patentable over Kovacevic et al. and Echeita et al.

Claim 9 recites that the first and second arbitration elements are synchronized. Kovacevic et al. and Echeita et al. do not disclose or suggest the combination of features recited in claim 9.

The Examiner alleged that Kovacevic et al. discloses first and second arbitration elements that are synchronized and cited column 8, lines 32-43, of Kovacevic et al. for support (Office Action, paragraph 10). Applicants respectfully disagree.

At column 8, lines 32-43, Kovacevic et al. discloses;

FIG. 9 illustrates the relationship between the various control and data signals of the transport stream. Specifically, FIG. 9 illustrates a TCLOCK signal having a rising edge for qualifying each data byte of the TDATA signal. Likewise, in the illustration of FIG. 9, the TVALID signal is always asserted during the first byte indicating that the data is valid. The TSTART signal is synchronized to the first byte of the TDATA signal, which is a synchronization byte. In a specific implementation, the synchronization byte of the TDATA signal will always have the Hexadecimal value 47h. The TERROR signal is not illustrated, however it would be asserted to indicate when an error has occurred.

This section of Kovacevic et al. discloses that a TSTART signal is synchronized to a first byte of a TDATA signal. Contrary to the Examiner's allegation, there is nothing in this section of Kovacevic et al. that discloses or remotely suggests first and second arbitration elements that are synchronized, where the first arbitration element arbitrates among the streams of variable speeds to store data in the memory and the second arbitration element arbitrates among the streams of variable speeds to read data from the memory, as required by claim 9.

The Examiner did not address these arguments when Applicants previously presented them. If the Examiner maintains the rejection of claim 9 based on Kovacevic et al., Applicants respectfully request that the Examiner identify where Kovacevic et al. or Echeita et al. discloses the features of claim 9 or identify claim 9 as allowable.

For at least these additional reasons, Applicants submit that claim 9 is patentable over Kovacevic et al. and Echeita et al.

Claim 10 recites features similar to features recited in claim 4, but with regard to the second arbitration element instead of the first arbitration element. Claim 10 is, therefore, patentable over Kovacevic et al. and Echeita et al. for at least reasons similar to reasons given with regard to claim 4. Claims 11 and 12 depend from claim 10 and are, therefore, patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claim 10. Further, claim 11 recites features similar to features recited in claim 5. Claim 11 is, therefore, also patentable over Kovacevic et al. and Echeita et al. for at least reasons similar to reasons given with regard to claim 5.

Independent claim 21 is directed to a method for processing data received in a plurality of incoming streams of variable speeds. The method comprises storing data from a plurality of

variable speed streams in a memory using a first arbitration element that arbitrates among the variable speed streams, and reading the data from the memory using a second arbitration element that arbitrates among the variable speed streams.

Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination, do not disclose or suggest the combination of features recited in claim 21. For at least reasons similar to reasons given with regard to claim 1, Kovacevic et al. and Echeita et al. do not disclose or suggest storing data from a plurality of variable speed streams in a memory using a first arbitration element that arbitrates among the variable speed streams, or reading the data from the memory using a second arbitration element that arbitrates among the variable speed streams.

For at least these reasons, Applicants submit that claim 21 is patentable over Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination. Claims 22-39 depend from claim 21 and are, therefore, patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claim 21. Claims 22-39 also recite features similar to features recited in claims 2-20. Claims 22-39 are, therefore, also patentable over Kovacevic et al. and Echeita et al. for at least reasons similar to reasons given with regard to claims 2-20.

Independent claim 40 is directed to a system for performing flow control on data in a plurality of incoming streams of variable speeds. The system comprises a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, a counter configured to determine a number of entries in the buffer corresponding to each of the streams, and a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream.

Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination, do not disclose or suggest the combination of features recited in claim 40. For example, Kovacevic et al. and Echeita et al. do not disclose or suggest a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries. As explained above with regard to claim 1, Kovacevic et al. and Echeita et al. are silent with regard to streams of variable speeds. Therefore, Kovacevic et al. and Echeita et al. cannot disclose or suggest a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, as required by claim 40.

The Examiner alleged:

As to applicant's argument one ordinary skill in the art at the time of the invention knows that the buffer is defined or in other word knows as temporarily storage where as in this case buffer is storing the video streams of variable length interpreted as plurality of streams of variable length.

(Office Action, paragraph 27). It appears that the Examiner is alleging that Kovacevic et al. discloses video streams of variable length and that video streams of variable length are equivalent to a plurality of streams of variable length. Even assuming, for the sake of argument that Kovacevic et al. discloses video streams of variable length (a point that Applicants do not concede), Applicants submit that claim 40 does not recite a plurality of streams of variable length, but instead recites a plurality of streams of variable speeds. Applicants submit that streams of variable length are different from streams of variable speeds.

Kovacevic et al. and Echeita et al. also do not disclose or suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds, as further recited in claim 40.

The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a prima facie case of obviousness with regard to claim 40.

When rejecting a similar feature in claim 16, however, the Examiner alleged that Kovacevic et al. discloses a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams and cited column 15, lines 45-62, of Kovacevic et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

At column 15, lines 45-62, Kovacevic et al. discloses:

At step 215, a determination is made whether the packet is a packet that is to be additionally parsed. For example, step 215 specifically indicates that a determination is being made whether the PID value indicates the packet is a video packet. If so, flow proceeds to step 226 for video parsing as indicated in FIG. 22. If the PID does not indicate a packet for special processing, i.e. not a video packet, the flow proceeds to step 227 where the data is sent to the buffer controller for storage, as indicated with reference to FIG. 22.

When the PID allocation table, or other means, indicates the packet is a video packet the Packetized Elementary Stream Parser (PESP) is enabled to allow further processing. In the specific embodiment of the PID allocation table listed above, the video PID is stored as PID_0. However, other methods of identifying the video PID, such as the use of a flag or other indicator are also possible. The operation of the PESP is controlled by the PESP Control Registers, as illustrated in FIG. 18.

Contrary to the Examiner's allegation, nowhere in this section, or any other section, does Kovacevic et al. disclose or remotely suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds, as required by claim 40.

Kovacevic et al. and Echeita et al. also do not disclose or suggest a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream, as further recited in claim 40.

The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting a similar feature in claim 16, however, the Examiner alleged that Kovacevic et al. discloses a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream and cited column 15, lines 45-62, of Kovacevic et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

Column 15, lines 45-62, of Kovacevic et al. is reproduced above. Contrary to the Examiner's allegation, nowhere in this section does Kovacevic et al. disclose or remotely suggest a comparator configured to determine whether to initiate flow control for each of the streams of variable speeds based on the determined number of entries for the stream, as required by claim 40.

At column 36, lines 37-46, however, Kovacevic et al. discloses that an interrupt can be generated to indicate that the video memory is ready to receive data, such as when the read pointer is at or past the watermark of the video memory. Nowhere in this section, or elsewhere, however, does Kovacevic et al. disclose or remotely suggest a comparator configured to determine whether to initiate flow control for each of the streams of variable speeds based on the determined number of entries for the stream, as required by claim 40.

For at least these reasons, Applicants submit that claim 40 is patentable over Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination. Claims 41-47 depend from claim 40 and are, therefore, patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claim 40.

Independent claims 48 and 55 recite features similar to, but possibly different in scope from, features recited in claim 40. Claims 48 and 55 are, therefore, patentable over Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given with regard to claim 40. Claims 49-54 depend from claim 48 and are, therefore, patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claim 48.

Independent claims 56 and 57 recite features similar to, but possibly different in scope from, features recited in claim 1. Claims 56 and 57 are, therefore, patentable over Kovacevic et al. and Echeita et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given with regard to claim 1.

New claims 58 and 59 depend from claim 1 and new claims 60 and 61 depend from claim 21. Claims 58-61 are, therefore, patentable over Kovacevic et al. and Echeita et al. for at least the reasons given with regard to claims 1 and 21.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-61.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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